Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Cancelled)

2. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit buffering said clock signal such that a logic low period and a logic high period of said clock signal are different from each other, wherein

said buffer circuit includes

a first inverter circuit receiving said clock signal and

a second inverter circuit receiving an output of said first inverter circuit,

one of said first and second inverter circuits including

a first transistor connected between a power supply node and an output node and having one polarity and

a second transistor connected between said output node and a ground node and having the other polarity, and a gate delay amount for an input signal at said first transistor and a gate delay amount for an input signal at said second transistor are different from each other.

3. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit buffering said clock signal such that a logic low period and a logic high period of said clock signal are different from each other, wherein

at least one of a power supply potential or a ground potential in said buffer circuit is different from another power supply voltage or ground voltage in said buffering portion.

4. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit buffering said clock signal such that a logic low period and a logic high period of said clock signal are different from each other, wherein

a substrate potential of a transistor included in said buffer circuit is different from a substrate potential of another transistor included in said buffering portion.

5. (Cancelled)

6. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal, said clock signal having a logic high period and a logic low period different from each other; and

a buffering portion buffering said clock signal, wherein

said frequency-multiplied circuit includes

a ring oscillator,

a comparator comparing a phase of said clock signal output from said ring oscillator with a phase of said reference clock signal,

a counter determining a digital count value based on a phase comparison result output from said comparator, and

a control circuit incrementing/decrementing said digital count value in response to a rising/falling of said clock signal,

said ring oscillator including a delay line varying a delay time in accordance with said digital count value.

7. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal, said clock signal having a logic high period and a logic low period different from each other; and

a buffering portion buffering said clock signal, wherein said frequency-multiplying circuit includes

a ring oscillator,

a comparator comparing a phase of said clock signal output from said ring oscillator with a phase of said reference clock signal, and

a counter determining a digital count value based on a phase comparison result output from said comparator,

said ring oscillator including

first and second delay lines connected in series for receiving said digital count value for determining a delay time, and

a selector selecting and outputting an input from one of said first and second delay lines in accordance with said clock signal.

8. (Original) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal;

a waveform generation circuit outputting a duty ratio control signal; and

an AND gate receiving said clock signal and said duty ratio control signal, wherein

in said duty ratio control signal, a period of time during which both of said clock signal and said duty ratio control signal are logic high is different from the other period of time.

9. (Original) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal;

a waveform generation circuit outputting a duty ratio control signal; and

an OR gate receiving said clock signal and said duty ratio control signal, wherein

in said duty ratio control signal, a period of time during which both of said clock signal and said duty ratio control signal are logic low is different from the other period of time.

10. (Cancelled)

11. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, wherein

said buffer circuit includes

a first inverter circuit receiving said clock signal, and

a second inverter circuit receiving an output of said first inverter circuit,

one of said first and second inverter circuits including

a plurality of first transistors connected in parallel between a power supply node and an output node and having one polarity,

a plurality of second transistors connected in parallel between said output node and a ground node and having the other polarity, and

a driving capability control portion controlling on/off of said plurality of first and second transistors respectively using a plurality of driving capability control signals.

12. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, wherein

said buffer circuit includes

a first inverter circuit receiving said clock signal,

a second inverter circuit receiving an output of said first inverter circuit, and

a timing control portion controlling rising or falling timing of a signal level output from said first inverter circuit to said second inverter circuit using a plurality of timing control signals.

13. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, wherein

at least one of a power supply potential and a ground potential of said buffer circuit varies using a control signal.

14. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, wherein

a substrate potential of a transistor included in said buffer circuit varies ~~can be varied~~ using a control signal.

15. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal,

said clock generation circuit further comprising:

a delay circuit capable of controlling a delay time using a delay control signal; and

a logic element receiving an output signal from said delay circuit and the reference clock signal for outputting a clock signal.

16. (Original) The clock generation circuit according to claim 15 wherein said logic element is an AND gate.

17. (Original) The clock generation circuit according to claim 15 wherein said logic element is an OR gate.

18. (Cancelled)

19. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said frequency-multiplying circuit is configured for changing a duty ratio of said clock signal, wherein

said frequency-multiplying circuit includes

a ring oscillator,

a comparator comparing a phase of said clock signal output from said ring oscillator with a phase of said reference clock signal,

a counter determining a digital count value based on a phase comparison result output from said comparator, and

a control circuit incrementing/decrementing said digital count value in accordance with a rising/falling of said clock signal when a count value control signal has a prescribed value,

said ring oscillator including a delay line varying a delay time in accordance with said digital count value.

20. (Original) The clock generation circuit according to claim 19 wherein

whether said count value control signal takes said prescribed value is determined in accordance with said digital count value.

21. (Original) The clock generation circuit according to claim 19 wherein

whether said count value control signal takes said prescribed value is determined in accordance with a frequency of said clock signal.

22. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said frequency-multiplying circuit is configured for changing a duty ratio of said clock signal, wherein

said frequency-multiplying circuit includes

a ring oscillator,

a comparator comparing a phase of said clock signal output from said ring oscillator with a phase of said reference clock signal,

a counter determining a digital count value based on a phase comparison result output from said comparator, and

a logic element receiving a selector control signal and said clock signal for outputting a select signal,

said ring oscillator including

first and second delay lines connected in series for receiving said digital count value for determining a delay time, and

a selector selecting and outputting an input from one of said first and second delay lines in accordance with said select signal.

23. (Original) The clock generation circuit according to claim 22 wherein whether said selector control signal takes said prescribed value is determined in accordance with said digital count value.

24. (Original) The clock generation circuit according to claim 22 wherein whether said selector control signal takes said prescribed value is determined in accordance with a frequency of said clock signal.

25. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal;

a waveform generation circuit generating a duty ratio control signal; and

an AND gate receiving said clock signal and said duty ratio control signal, wherein

in said duty ratio control signal, a ratio between a period of time during which both of said clock signal and said duty ratio control signal are logic high and the other period of time varies.

26. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal;

a waveform generation circuit generating a duty ratio control signal; and

an OR gate receiving said clock signal and said duty ratio control signal, wherein

in said duty ratio control signal, a ratio between a period of time during which both of said clock signal and said duty ratio control signal are logic low and the other period of time varies.

Claims 27-54. (Cancelled)

55. (Previously Presesnted) A system comprising:

a clock generation circuit outputting a clock signal;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal; and

a central processing unit controlling said clock controlling circuit,

said clock generation circuit including

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting said clock signal same as or multiplied in frequency of said reference clock signal, and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, said system further comprising

a current measurement circuit measuring an operating current of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said operating current.

56. (Previously Presented) A system comprising:

a clock generation circuit outputting a clock signal;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal; and

a central processing unit controlling said clock controlling circuit,

said clock generation circuit including

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting said clock signal same as or multiplied in frequency of said reference clock signal, and

a buffering portion buffering said clock signal, wherein

said frequency-multiplying circuit is configured for changing a duty ratio of said clock signal,

said system further comprising

a current measurement circuit measuring an operating current of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said operating current.

57. (Previously Presented) A system comprising:

the clock generation circuit according to claim 25;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal;

a central processing unit controlling said clock controlling circuit; and

a current measurement circuit measuring an operating current of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said operating current.

58. (Previously Presented) A system comprising:

the clock generation circuit according to claim 26;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal;

a central processing unit controlling said clock controlling circuit; and

a current measurement circuit measuring an operating current of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said operating current.

59. (Previously Presented) A system comprising:

a clock generation circuit outputting a clock signal;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal; and

a central processing unit controlling said clock controlling circuit,

said clock generation circuit including

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting said clock signal same as or multiplied in frequency of said reference clock signal, and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal,

said system further comprising

a temperature measurement circuit measuring a temperature of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said temperature.

60. (Previously Presented) A system comprising:

a clock generation circuit outputting a clock signal;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal; and

a central processing unit controlling said clock controlling circuit,

said clock generation circuit including

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting said clock signal same as or multiplied in frequency of said reference clock signal, and

a buffering portion buffering said clock signal, wherein

said frequency-multiplying circuit is configured for changing a duty ratio of said clock signal,

said system further comprising

a temperature measurement circuit measuring a temperature of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said temperature.

61. (Previously Presented) A system comprising:

the clock generation circuit according to claim 25;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal;

a central processing unit controlling said clock controlling circuit; and

a temperature measurement circuit measuring a temperature of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said temperature.

62. (Previously Presented) A system comprising:

the clock generation circuit according to claim 26;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal;

a central processing unit controlling said clock controlling circuit; and

a temperature measurement circuit measuring a temperature of a circuit receiving said clock signal, wherein

said central processing unit controls a duty ratio of said clock signal or on/off of duty ratio control based on a measurement result of said temperature.

Claims 63-74. (Cancelled)

75. (Previously Presented) A system comprising:

a clock generation circuit outputting a clock signal;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal; and

a central processing unit controlling said clock controlling circuit,

said clock generation circuit including

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting said clock signal same as or multiplied in frequency of said reference clock signal, and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, said system further comprising

a module circuit receiving said clock signal for operation, wherein

a duty ratio of said clock signal can be set by an instruction from said central processing unit, individually for said clock signal being supplied to said module circuit and for said clock signal being supplied to a prescribed external circuit.

76. (Previously Presented) A system comprising:

a clock generation circuit outputting a clock signal;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal; and

a central processing unit controlling said clock controlling circuit,

said clock generation circuit including

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting said clock signal same as or multiplied in frequency of said reference clock signal, and

a buffering portion buffering said clock signal, wherein

said frequency-multiplying circuit is configured for changing a duty ratio of said clock signal,

said system further comprising

a module circuit receiving said clock signal for operation, wherein

a duty ratio of said clock signal can be set by an instruction from said central processing unit, individually for said clock signal being supplied to said module circuit and for said clock signal being supplied to a prescribed external circuit.

77. (Previously Presented) A system comprising:

the clock generation circuit according to claim 25;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal;

a central processing unit controlling said clock controlling circuit; and

a module circuit receiving said clock signal for operation, wherein

a duty ratio of said clock signal can be set by an instruction from said central processing unit, individually for said clock signal being supplied to said module circuit and for said clock signal being supplied to a prescribed external circuit.

78. (Previously Presented) A system comprising:

the clock generation circuit according to claim 26;

a clock controlling circuit controlling a duty ratio of said clock signal using a control signal;

a central processing unit controlling said clock controlling circuit; and

a module circuit receiving said clock signal for operation, wherein

a duty ratio of said clock signal can be set by an instruction from said central processing unit, individually for said clock signal being supplied to said module circuit and for said clock signal being supplied to a prescribed external circuit.

79. (Previously Presented) A clock generation circuit comprising:

a frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal; and

a buffering portion buffering said clock signal, wherein

said buffering portion includes at least one buffer circuit for changing a duty ratio of said clock signal, wherein

said frequency-multiplying circuit includes

a ring oscillator,

a comparator comparing a phase of said clock signal output from said ring oscillator with a phase of said reference clock signal,

a counter determining a digital count value based on a phase comparison result output from said comparator, and

a control circuit incrementing/decrementing said digital count value in accordance with a rising/falling of said clock signal when a count value control signal has a prescribed value,

said ring oscillator including a delay line varying a delay time in accordance with said digital count value.